AMENDMENTS TO THE CLAIMS

1. (original) A method for forming a structure for testing external connections to semiconductor devices, the method comprising:
providing a thin film of electrically insulating material;
providing a plurality of passages through the thin film of electrically insulating material, wherein the passages are arranged in a pattern corresponding to a pattern of external connections on the semiconductor device;
providing electrically conducting material in the plurality of passages; and
providing electrical connections between the electrically conducting material in selected passages.

2. (original) The method according to claim 1, wherein providing the electrical connections between the electrically conducting material in the selected passages comprises providing electrically conducting material on the thin film of electrically insulating material between the selected passages.

3. (original) The method according to claim 1, wherein the selected passages are adjacent pairs.

4. (original) The method according to claim 1, wherein the electrical connections are provided between a plurality of passages.

5. (Currently amended) The method according to claim 1, wherein the electrical connections are provided between non-adjacent passages.

6. (new) A structure for testing external connections to semiconductor devices, the structure comprising:
an external electrical path between selected external connections on the semiconductor devices.

7. (new) The structure according to claim 6, wherein the external electrical path comprises a thin film interface probe.

8. (new) The structure according to claim 6, wherein the external electrical path permits a driver from an input/output to interface to a receiver of a corresponding paired input/output.

9. (new) The structure according to claim 6, wherein the external connections on the semiconductor devices are C4 connections.

10. (new) The structure according to claim 6, wherein the structure carries out boundary scan and input/output wrap test techniques.

11. (new) The structure according to claim 6, wherein all adjacent input/output pairs are paired.

12. (new) The structure according to claim 6, wherein the structure provides a high frequency closed loop self test of drivers and receivers.

13. (new) The structure according to claim 6, wherein the structure is extendible to full wafer contacting for burn-in and test.

14. (new) The structure according to claim 6, wherein the external electrical path comprises:
a thin film of electrically insulating material;
a plurality of passages through the thin film of electrically insulating material, wherein the passages are arranged in a pattern corresponding to a pattern of external connections on the semiconductor device;
electrically conducting material arranged in the plurality of passages; and
electrical connections between the electrically conducting material in selected pairs of the plurality of passages.

15. (new) The structure according to claim 14, further comprising:
a space transformer connected to the electrically conducting material arranged in the plurality of passages.

16. (new) The structure according to claim 6, wherein the external electrical path is provided between pairs of external connections on the semiconductor devices.

17. (new) The structure according to claim 6, wherein the external electrical path is provided between a plurality of external connections on the semiconductor devices.

18. (new) The structure according to claim 6, wherein the external electrical path is provided between non-adjacent external connections on the semiconductor devices.